Electronic Version
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Claims

[c1] What is claimed is:

1.A method for accessing data of a computer system, the computer system comprising:

a first memory;

a second memory;

an address decoder;

a digital signal processing unit electrically connected to the address decoder;

a demultiplexer having an input end electrically connected to the digital signal processing unit, a first output end electrically connected to the second memory, and a control end electrically connected to the address decoder; and

a multiplexer having an output end electrically connected to the digital signal processing unit, a first input end electrically connected to the second memory, and a control end electrically connected to the address decoder; and

the method comprising following steps:

(a)providing the digital signal processing unit with a cache memory electrically connected to the first memory, the cache memory having an input end electrically con-

nected to a second output end of the demultiplexer, an output end electrically connected to a second input end of the multiplexer, and a tag stored with an address data; and

(b)when the digital signal processing unit generates an address signal, (c) controlling the demultiplexer with the address decoder according to the address signal to transfer the address signal either to the cache memory or to the second memory and to enable the digital signal processing unit to receive contents via the multiplexer either from the cache memory or from the second memory, (d) comparing the address signal with the address data if the address signal is transmitted to the cache memory, and either transmitting contents of the cache memory corresponding to the address signal via the multiplexer to the digital signal processing unit if the address signal matches the address data or updating contents of the cache memory corresponding to the address signal with contents of the first memory corresponding to the address signal, (e) updating the address data with the address signal and transmitting the updated contents of the cache memory via the multiplexer to the digital signal processing unit, and (f) transmitting contents of the second memory corresponding to the address signal via the multiplexer to the digital signal processing unit if the address signal is transmitted to the

second memory.

[c2] 2.The method of claim 1 wherein the address decoder, the second memory, the digital signal processing unit, the demultiplexer, the multiplexer, and the cache memory are all integrated into a digital signal processing chip.

[c3] 3.The method of claim 1 wherein the first memory is a dynamic random access memory (DRAM).

[c4] 4.The method of claim 1 wherein the second memory is a static random access memory (SRAM).

[c5] 5.A computer system comprising:
a first memory;
a second memory;
an address decoder;
a digital signal processing unit electrically connected to the address decoder;
a demultiplexer having an input end electrically connected to the digital signal processing unit, a first output end electrically connected to the second memory, and a control end electrically connected to the address decoder;
a multiplexer having an output end electrically connected to the digital signal processing unit, a first input

end electrically connected to the second memory, and a control end electrically connected to the address decoder; and

a cache memory having an input end electrically connected to a second output end of the demultiplexer, an output end electrically connected to a second input end of the multiplexer, and a tag for storing an address.

[c6] 6.The computer system of claim 5 wherein the address decoder, the second memory, the digital signal processing unit, the demultiplexer, the multiplexer, and the cache memory are all integrated into a digital signal processing chip.

[c7] 7.The computer system of claim 5 wherein the first memory is a DRAM.

[c8] 8.The computer system of claim 5 wherein the second memory is an SRAM.